Compact LNA and VCO 3-D MMICs Using Commercial GaAs PHEMT Technology for V-band Single-chip TRX MMIC

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Abstract — **This paper presents compact V-band low-noise amplifier (LNA) and Ka-band voltage-control oscillator (VCO) 3-D MMICs for a V-band highly-integrated single-chip transceiver MMIC. 3-D MMICs are fabricated through the cooperation of commercial foundry GaAs pHEMT and 3-D interconnection processes. The LNA (chip size is 0.75 mm^2) achieves 15 dB gain and better than 3.3 dB noise figure from 50 GHz to 60 GHz. The VCO (chip size of 0.52 mm^2) achieves 11.5 dBm output power, 3.8 GHz oscillation frequency tuning range, and a phase noise of -102 dBc/Hz at 1 MHz offset and 28.6 GHz output signal. The cooperation 3-D MMIC technology with a high-performance commercial foundry technology promises low-cost, compact, and high performance millimeter-wave MMICs.**

I. INTRODUCTION

The strong demands for high-speed wireless applications have stimulated the development of low cost and compact millimeter-wave wireless equipment for use of millimeter-wave frequencies. V-band applications are very interesting for their higher transmission rates based on the wider bandwidths possible. For these applications, a single-chip transceiver configuration that is very compact is desired since this structure eliminates the complex packaging process, resulting in low cost compact equipment.

Authors have proposed and demonstrated the three-dimensional (3-D) MMIC technology [1], which greatly reduces circuit area and so offers low-cost MMICs. Furthermore, the 3-D MMIC technology can realize high-level integration on a single-chip, resulting in a significant reduction in millimeter-wave packaging cost and manufacturing time. A cost-effective MMIC development method based on the 3-D MMIC concept, which involves the cooperation of device foundries and 3-D/multilayer interconnection process foundries, has been proposed [2]. The proposed method reduces the development time, and eases the risk of new device development since the device process is segregated from the interconnect process. The designers have excellent flexibility in choosing the device and the interconnection processes to suit their applications, while the foundries can focus on the development of their specialized technologies.

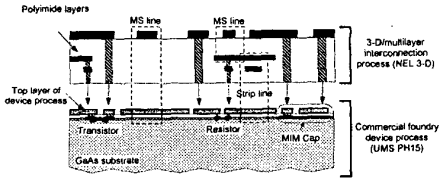

Fig. 1. Structure of 3-D MMIC fabricated by combining commercial foundry process with 3-D MMIC interconnection process.

This paper presents a newly developed compact V-band low-noise amplifier (LNA) and a Ka-band voltage control oscillator (VCO) for a V-band single-chip transceiver MMIC. The MMICs were fabricated by combining a commercial 0.15 μm GaAs pHEMT process with the 3-D MMIC interconnection process based on the proposed development method. These MMICs can be simply integrated with other components on the same chip to realize a V-band single-chip transceiver MMIC. Our proposed methodology, based on the 3-D MMIC technology, promises to greatly reduce the cost and development time of millimeter-wave equipment.

II. FABRICATION PROCESS

Fig. 1 illustrates the structure of the 3-D MMIC combined with a commercial foundry device. We combined a commercial 0.15 μm GaAs pHEMT foundry process (UMS PH15) from United Monolithic Semiconductor S.A.S. (UMS) with the 3-D MMIC interconnection process from NTT Electronics Corp. (NEL) that originated in NTT Laboratories [3]. The 3-D MMIC interconnection layer, which consists of four layers of 2.5-μm polyimide film, was formed on PH15 GaAs wafers delivered by UMS. Surface roughness of the wafer is effectively absorbed by the polyimide film, resulting in a 3-D MMIC structure with uniform thickness. We evaluated PH15 device performance before and after the 3-D MMIC interconnection process. This evaluation of the device before the 3-D MMIC process enabled us to modify

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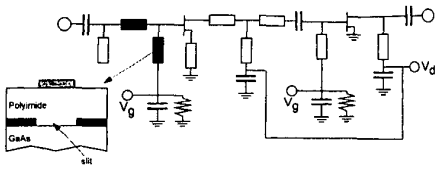


Fig. 2. Equivalent circuit of fabricated LNA 3-D MMIC.

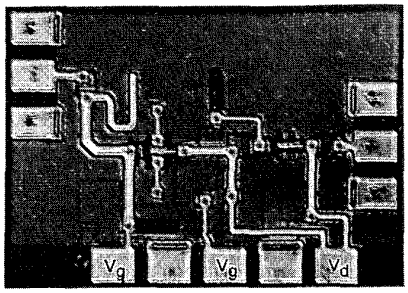


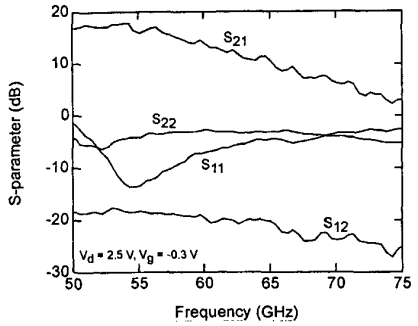
Fig. 3. Microphotograph of fabricated LNA 3-D MMIC.

passive MMIC circuits to obtain the best performances by using real device parameters. The final transistor performance after the 3-D MMIC process achieves an f_T of 110 GHz and an f_{max} of 170 GHz despite the increase in parasitic capacitance in the transistor due to formed polyimide film.

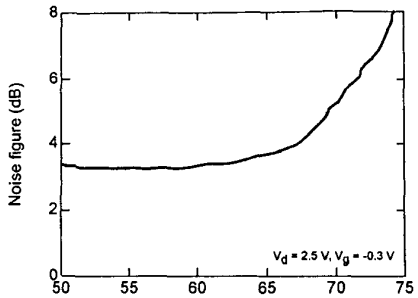
III. V-BAND LNA

An equivalent circuit of the fabricated two-stage LNA is shown in Fig. 2. The LNA consists of two 2 x 50-μm gate-width pHEMT devices, TFMS lines, and low-loss TFMS lines with a ground slit (see Fig. 2). The loss of the TFMS line with the ground slit (Z_0 = 50 Ω, w = 30 μm, slit gap = 30 μm) is 40% less than that of the normal TFMS line (Z_0 = 50 Ω, w = 22 μm). The transistor model used considered the parasitic capacitance of the 3-D structure. The input matching circuit was optimized to achieve low-noise performance. Inter section and output matching circuits were simplified to obtain compactness. Fig. 3 shows a microphotograph of the fabricated LNA MMIC. The intrinsic area of this LNA is just 0.73 mm x 0.46 mm (chip size is 1.04 mm x 0.72 mm).

Measured performances of the fabricated MMIC are shown in Fig. 4. The MMIC achieves a gain of 15.5 dB ± 1.5 dB and a noise figure of better than 3.3 dB from 50 GHz to 60 GHz. The input and output return losses are 8 dB and 3 dB at 60 GHz, respectively. Drain and gate biases are 2.5 V and -0.3 V, respectively, and the power consumption is 62 mW.



(a)



(b)

Fig. 4. Measured performances of fabricated LNA. (a) S-parameter, (b) Noise figure

Fig. 5 plots the state-of-the-art of reported V-band LNA MMICs [4]-[7] using InP HEMT, GaAs HEMT, and GaAs MESFET structure. This figure also shows the performance of microstrip (MS), coplanar waveguide (CPW), and 3-D MMIC configurations. The noise figure performance of the fabricated 3-D MMIC LNA is competitive with the other GaAs pHEMT MMIC LNAs, while the gain density of the fabricated MMIC is about 50, which is 3 times higher than the top performance achieved by conventional MMICs.

IV. KA-BAND VCO

Fig. 6 shows the circuit diagram of the fabricated Ka-band VCO MMIC. The VCO is based upon a common-source series feedback topology. The active pHEMT

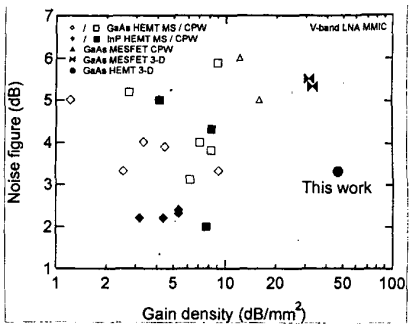


Fig. 5. Noise figure performance of V-band 3-D MMIC LNA.

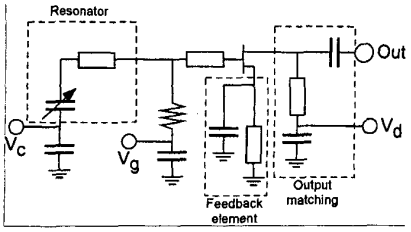


Fig. 6. Equivalent circuit of fabricated VCO 3-D MMIC.

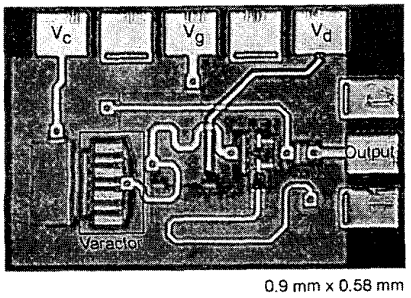


Fig. 7. Microphotograph of fabricated VCO 3-D MMIC.

device has 4 x 30 μm gate width. The drain-source shorted pHEMT device with 6 x 50 μm gate width was implemented as a variable capacitance that provides oscillation frequency tuning. The feedback section used to generate instability consists of a short stub in parallel with a small capacitance. The resonance section consists of a 70-Ω TFMS line in series with a variable capacitance that provides low series resistance. The output matching circuit was simplified to realize compactness. Fig. 7 shows a microphotograph of the fabricated VCO MMIC. The intrinsic area is just 0.68 mm x 0.38 mm (chip size is 0.9 mm x 0.58 mm).

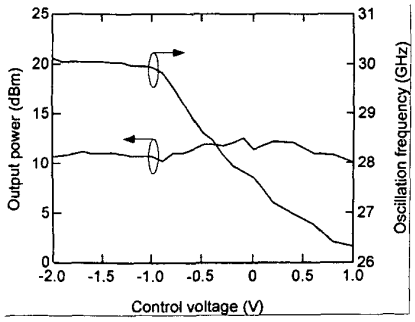


Fig. 8. Measured output power and oscillation frequency.

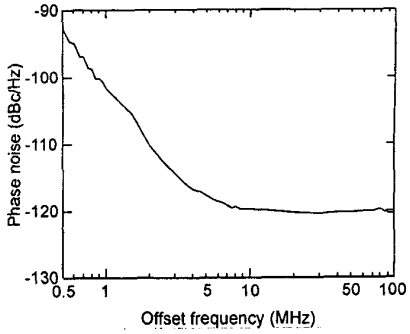


Fig. 9. Measured SSB phase noise.

Fig. 8 shows measured output power and oscillation frequencies versus the control voltage applied on the variable capacitance. Measured oscillation frequencies are 26.3 GHz to 30.1 GHz; the tuning range is 3.8 GHz at a control bias of -2 V to 1 V. The corresponding output power is 11.3 dBm ± 1.2 dBm in the oscillation frequency tuning range. The center oscillation frequency is 28.2 GHz with an output power of 11.8 dBm. The drain and gate biases are 2.5 V and 0 V, respectively. Fig. 9 shows measured single-side band (SSB) phase noise performance at the control bias of -0.5 V on the variable capacitance. This measurement was performed by using a spectrum analyzer. The phase noise achieves -102 dBc/Hz at 1 MHz offset.

Table I compares the performances of reported Ka-band VCO MMICs. The developed VCO MMIC offers competitive performance and significantly improved tuning range and reduced chip size.

V. CONCLUSION

This paper demonstrates ultra compact V-band LNA and VCO 3-D MMICs fabricated by combining a commercial GaAs pHEMT process with the 3-D MMIC interconnection process. The fabricated LNA MMIC achieves 15 dB gain and 3.3 dB noise figure on a chip that is 0.75 mm^2. The fabricated VCO MMIC also achieves 11.3 dBm output power with a frequency tuning range of 3.8 GHz and a phase noise of -102 dBc/Hz at 1 MHz offset on a chip that is 0.52 mm^2. The developed compact MMICs are key elements to construct a transceiver MMIC, and effectively support integration to form a the single-chip transceiver MMIC. In addition, the cooperation of the commercial GaAs pHEMT foundry process with the 3-D MMIC interconnection process promises high performance MMICs at very low cost.

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TABLE I

STATE-OF-THE-ART OF KA-BAND VCO GAAS MMIC

Technology	Chip size (mm^2)	Center osc. freq. (GHz)	Tuning range (GHz)	Output power at center freq. (dBm)	Phase noise @ 100 kHz offset (dBc/Hz)	Phase noise @ 1 MHz offset (dBc/Hz)	Ref.
0.25 μm MESFET	3	38.25	0.5	12	-75	-95	[8]
0.25 μm HEMT	3.5	29.85	2.3	11	-70	-	[9]
0.2 μm HEMT	4	29.6	1.2	12	-	-	[10]
0.2 μm pHEMT	3.2	38.45	2.4	0	-63	-	[11]
0.2 μm pHEMT	2.25	33.75	0.35	9.4	-	-	[12]
0.18 μm pHEMT	-	29.3	0.55	0	-62	-	[13]
0.15 μm pHEMT	**0.5**	**28.2**	**3.8**	**11.8**	**-**	**-102**	**This work**
InGaP/GaAs HBT	-	36.75	1.1	2.3	-80	-107	[14]
InAlAs/InGaAs HBT	3.2	38.4	0.85	10 (with amp.)	-82	-107	[15]